



Substitute for form 1449A/PTO			Complete if Known		
			Application Number	09/881934	
INFORMATION DISCLOSURE STATEMENT BY APPLICANT (use as many sheets as necessary)			Filing Date	06/14/01	
			First Named Inventor	ENRIQUE MUSOLL	
			Group Art Unit	2188	
			Examiner Name	KEVIN L. ELLIS	
			Attorney Docket Number	MIPS.0173-00-US	
Sheet	1	of	1		

U.S. PATENT DOCUMENTS					
Examiner Initials*	Cite No. ¹	Document Number	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
		Number-Kind Code ² (if known)			
UR		US-5784649	07-21-1998	BEGUR ET AL.	
		US-6529515	03-04-2003	RAZ ET AL.	
		US-6640248	10-28-2003	JORGENSEN, JACOB W.	
		US-6625808	09-23-2003	TARDITI, DAVID R.	
		US-6738371	05-18-2004	AYRES, LAWRENCE	
		US-6738378	5-18-2004	TUCK, III; RUSSELL R.	
UR		US-6813268	11-02-2004	KALKUNTE ET AL.	
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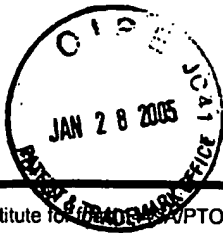
FOREIGN PATENT DOCUMENTS						
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Examiner Signature	Kevin L. Ellis	Date Considered	3/16/05
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Substitute for Information Disclosure Statement by Applicant INFORMATION DISCLOSURE STATEMENT BY APPLICANT (use as many sheets as necessary)			Complete if Known		
			Application Number	09/881934	
			Filing Date	02/13/04	
			First Named Inventor	ENRIQUE MUSOLL	
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UR		US-5708814	01-13-1998	SHORT ET AL.	
		US-5724565	03-13-1998	DUBEY ET AL.	
		US-5784699	07-21-1998	MCMAHON ET AL.	
		US-6460105	10-01-2002	JONES ET AL.	
		US-6523109	02-18-2003	MEIER, STEPHAN G.	
		US-20010004755	06-21-2001	LEVY ET AL.	
		US-20020049964	04-25-2002	TAKEYAMA ET AL.	
UR		US-20020071393	06-13-2002	ENRIQUE MUSOLL	
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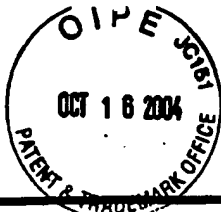
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UR	AA	WO 03/005645A2	01-16-2003	SAMPATH ET AL.		

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NR		US-4200927	04-29-1980	Hughes et al.	
NR		US-6535905	03-18-2003	Kalafatis et al.	
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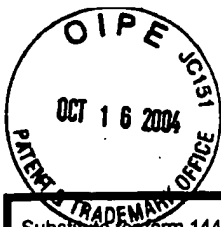
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NON PATENT LITERATURE DOCUMENTS			
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UR	AA	YAMAMOTO, WAYNE. <i>An Analysis of Multistreamed, Superscalar Processor Architectures</i> . University of California Santa Barbara Dissertation. December 1995. Santa Barbara, US.	
	AB	YAMAMOTO et al. "Increasing Superscalar Performance Through Multistreaming." <i>Parallel Architectures and Compilation Techniques (PACT '95)</i> . 1995	
	AC	<i>The PowerPC Architecture: A Specification for a New Family of RISC Processors</i> . 2 nd Ed. May 1994. pp. 70-72. Morgan Kaufmann. San Francisco, US.	
	AD	<i>MC68020 32-Bit Microprocessor User's Manual</i> . 3 rd Ed.. 1989. pp. 3-125, 3-126, and 3-127. Prentice Hall, NJ, US.	
	AE	POTEL, M. J. "Real-Time Playback in Animation Systems." <i>Proceedings of the 4th Annual Conference on Computer Graphics and Interactive Techniques</i> . 1977. pp. 72-77. San Jose, CA, US.	
	AF	<i>ARM Architecture Reference Manual</i> . 1996. pp. 3-41, 3-42, 3-43, 3-67, and 3-68. Prentice Hall, NJ, US.	
	AG	<i>ESA/390 Principles of Operation</i> . IBM Online Publications Center Reference Number SA22-7201-08. Table of Contents and paras. 7.5.31 and 7.5.70. IBM Corporation. Boulder, CO, US.	
	AH	<i>MC88110 Second Generation RISC Microprocessor User's Manual</i> . 1991. pp. 10-66, 10-67, and 10-71. Motorola, Inc.	
	AI	DIEFENDORFF, KEITH ET AL. "Organization of the Motorola 88110 Superscalar RISC Microprocessor." <i>IEEE Journal of Microelectronics</i> . April 1992. pp. 40-63. Vol. 12, No. 2. IEEE. New York, NY, US.	
	AJ	KANE, GERRY. <i>PA-RISC 2.0 Architecture</i> . 1996, pp. 7-106 and 7-107. Prentice Hall. NJ, US.	
	AK	DIEFENDORFF, KEITH ET AL. "Altivec Extension to PowerPC Accelerates Media Processing." <i>IEEE Journal of Microelectronics</i> . Vol. 20, No. 2 (2000): pp. 85-95	
	AL	GRUNEWALD, WINFRIED ET AL. "Towards Extremely Fast Context Switching in a Block Multithreaded Processor." <i>Proceedings of EUROMICRO 22</i> , 1996. pp. 592-599	
	AM	BRADFORD, JEFFREY ET AL. "Efficient Synchronization for Multithreaded Processors." <i>Workshop on Multithreaded Execution, Architecture, and Compilation</i> . Jan-Feb 1998. pp. 1-4	
UR	AN	PAI, VIJAY ET AL. "An Evaluation of Memory Consistency Models for Shared-Memory Systems with ILP Processors." <i>Proceedings of ASPLOS-VII</i> , Oct. 1996: pp. 12-23, ACM, Inc.	

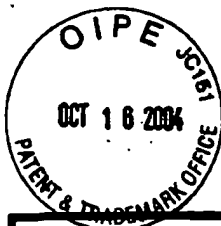
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UR	AO	YOA ET AL. "Speculation Techniques for Improving Load Related Instruction Scheduling." 1999. Pages 42-53, IEEE.	
	AP	KESSLER, R. E. "The Alpha 21264 Microprocessor: Out-of-Order Execution at 600 MHz." August 1998.	
	AQ	DONALDSON ET AL. "DISC: Dynamic Instruction Stream Computer, An Evaluation of Performance." 26 th Hawaii Conference on Systems Sciences. Vol. 1. 1993. Pages 448-456.	
	AR	NEMIROVSKY ET AL. "DISC: Dynamic Instruction Stream Computer." ACM. 1991. Pages 163-171	
	As	MUSOLL ET AL., "Mechanism to Activate a Context When No Stream is Running in a Multi-Streaming Processing Core," April 16, 2001, Disclosure Document #492431, USPTO	
	AT	MUSOLL ET AL., "Mechanism for Allowing a Limited Packet Head and/or Tail Growth Without Moving the Packet to a Different Memory Location," April 16, 2001, Disclosure Document #492429, USPTO	
	AU	MUSOLL, ENRIQUE, "Functional Validation of a Packet Management Unit," May 18, 2001, Disclosure Document #494011, USPTO	
	AV	MELVIN ET AL., "Extended Instruction Set for a Packet Processing Applications," July 5, 2001, Disclosure Document #496559, USPTO	
UR	AW	MUSOLL ET AL., "Mechanism to Overflow Packets to a Software Controlled Memory When They Do Not Fit into a Hardware Controlled Memory," July 3, 2001, Disclosure Document #496391, USPTO	

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